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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G06F 9/318, 9/30 — A1

(11) International Publication Number: **WO 00/19311**

(43) International Publication Date: 6 April 2000 (06.04.00)

(21) International Application Number: PCT/US99/22551

(22) International Filing Date: 30 September 1999 (30.09.99)

(30) Priority Data:
09/163,741 30 September 1998 (30.09.98) US

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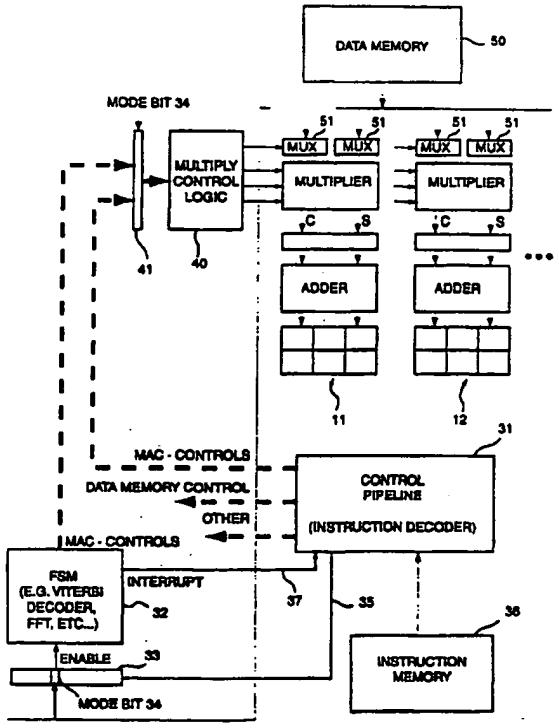
(81) Designated States: CA, JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD FOR DYNAMIC ALLOCATION AND SHARING OF FUNCTIONAL UNIT DATAPATHS

(57) Abstract

The invention is a processing method and a processor architecture which contains multiple processors on the same silicon but which does not make a fixed compromise by statically assigning processing units to the processors but rather dynamically assigns such processing units so that they may be efficiently shared. The invention may provide the same functionality as was obtained with static allocation, and may be implemented on a single chip with much lower area for the same level of performance. The preferred architecture uses a mode bit that may be programmatically set for passing control from a general purpose instruction decoder to a finite state machine. The preferred architecture further includes a multiplexer that uses the mode bit as its selection input.



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METHOD FOR DYNAMIC ALLOCATION AND SHARING OF FUNCTIONAL UNIT DATAPATHS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates generally to data processing structures and methods therefore and, more particularly, to a data processing architecture wherein alternative control mechanisms (i.e. an instruction-decoder and a specialized state machine) may be dynamically bound to a shared functional unit or group of functional units.

DESCRIPTION OF RELATED ART

Microprocessors form a critical component of modern electronic devices. Various microprocessor architectures have developed, depending on the intended use of the device. All microprocessors, however, are based around one or more "functional units" or data path circuits that perform a specified operation such as an add function, a subtract function, a shift by one, and so on. The universe of functional units can generally be divided into two varieties: (1) general purpose functional units that may be programmatically controlled by way of an instruction stream and a suitable instruction-decoder and (2) special purpose functional units that are typically optimized to perform a single function (e.g. a multiply) and are typically controlled by a specialized finite state machine (FSM).

Viewing microprocessors as comprising functional units, one can logically see a range of available architectures that extends from a completely general architecture to a completely dedicated architecture. The Pentium processor made by Intel is an example of a completely general architecture, which does not contain any special purpose, dedicated functional units, but rather a plurality of general purpose functional units that are all controlled by an instruction pipeline. The advantage of such a general purpose processor is that all of the functional units are always available for use. Such generality, however, comes at the cost of size and performance because there is an inherently inefficient use of the microprocessors resources.

At the other end of the spectrum are fixed functionality microprocessors that contain only dedicated, special purpose functional units that are controlled by finite state machines. An integrated circuit designed to implement the MPEG-2 video compression standard, for example, is likely to contain such dedicated functional units and strict FSM control because it implements a very limited function.

In between the two extremes or paradigms, various industry members have designed and implemented microprocessors that incorporate both general purpose functional units controlled by an instruction stream, and special purpose functional units controlled by a finite state machine. In all known cases, however, such mixed-functionality microprocessors have implemented a static division or compromise between the two control mechanisms, i.e. between an instruction stream and corresponding instruction-decoder on one hand, and one or more finite state machines on the other hand. The functional units available for control by the various control mechanisms, in other words, are dedicated to those control mechanisms. In the known prior art therefore, the industry has either selected one of the extreme paradigms or has made a compromise that was, in some cases, a fixed compromise. A functional unit takes data out of memory, operates on that data, and then puts the result back in memory. A

control unit tells the functional unit what data to use or provides the functional unit with that data, depending on the point of view.

Microprocessors on the specialized end of the spectrum are often referred to as digital signal processors or DSPs. DSPs are often used in special purpose electronic devices such as, for example, wireless communication devices (cellular and portable phones) and modems. The DSPs in such devices often implement mathematically intensive algorithms such as Viterbi decoding, REED-SOLOMON decoding, and Fast Fourier Transforms, to name a few.

The processor architectures which have made a fixed compromise between general purpose and specialized functional units and appropriate control therefore have generally achieved their intended purpose of merging general purpose functionality with specialized, high speed data processing functionality. Such devices, however, are inefficient in that the various functional units, which must be provided to achieve the static compromise, are often idle when the processor executes multiple applications. The result of the static compromise, therefore, is a larger than necessary die-size, a more costly processor, additional power consumption, reduced speed and depending on other limiting issues, restricted applicability to new applications.

There remains a need, therefore, for a processor architecture which will efficiently combine the structures and resulting benefits of general purpose functional units and specialized functional units in such a way that they may be dynamically shared between two or more control mechanisms.

SUMMARY OF THE INVENTION

In one aspect, the invention may be regarded as a method of dynamically sharing a processing unit between multiple control mechanisms, the method comprising the steps of: providing a processing unit; providing an instruction decoder for executing a first program

stored in a memory; providing a finite state machine for executing a second program according to the finite state machine; and dynamically assigning the processing unit to the instruction decoder and the finite state machine in accordance with the first and second programs.

In another aspect, the invention may be regarded as a multiprocessor IC comprising: a processing unit; a control pipeline including an instruction decoder and an output for issuing control signals to the processing unit; a finite state machine including an output for issuing control signals to the processing unit; and means for dynamically assigning the control signals from the instruction decoder and the control signals from the finite state machine to the processing unit.

BRIEF DESCRIPTION OF THE DRAWINGS

The just summarized invention may be best understood with reference to the drawings of which

Figure 1 is a high level diagram showing how a data path-pool of functional units that communicate with a memory-pool may be dynamically controlled by two or more control mechanisms such as a finite state machine or an instruction-decoder contained in the control-pool; and

Figure 2 is a schematic block diagram of a first preferred embodiment involving a dynamic control sharing arrangement between an instruction-decoder and one or more finite state machines.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In modern electronic devices, general purpose system control is implemented with appropriate firmware, an instruction decoder, and one or more general purpose execution

units. In addition, however, it is often the case that certain functions must be implemented at very high speed and performance levels. In certain communications devices, for example, equalization, echo cancellation, Viterbi encoding and decoding, and so on, must generally be implemented with finite state machines that control more specialized functional units such as multipliers, adders, and multiply-accumulators (MACs).

The goal of this invention is to dynamically allocate processing units (execution units; functional units, or both) among two or more control mechanisms on a chip that has one or more general purpose processors or digital signal processors controlled by an instruction stream and one or more algorithm accelerators controlled by a finite state machine (FSM). The dynamic allocation approach is proposed instead of statically predetermining the division of resources on the chip as has been done in the past. In such context, the application developer may simply decide at run-time what resources will be used to implement a particular task. The result of this invention is the more efficient use of available on-chip resources. Consequently, the same functionality may be implemented on a single chip with much lower area and power for the same level of performance.

Figure 1 is a high level diagram showing how a pool 10 of data paths DP1, DP2, or functional units, that communicate with a memory-pool 20 may be dynamically controlled by a control pool 30 of two or more control mechanisms such as a finite state machine FSM and an instruction-decoder. The invention here is to dynamically assign any one of the various control mechanisms in the control pool 30 to the functional units DP1, DP2 in the datapath pool 10.

Figure 2 is a schematic block diagram of a first preferred embodiment involving a dynamic control-sharing arrangement for sharing functional units 11, 12, and so on, between a control pipeline 31 containing an instruction-decoder and a finite state machine (FSM) 32. As shown, the preferred dynamic sharing arrangement is based around a control register 33

which includes a "mode bit" 34 that the firmware may programmatically set, as suggested by control line 35, to pass control to or "enable" the FSM 32.

The system of Figure 2 operates as follows. Assuming that the control pipeline 31 has control of the functional units 11, 12, then firmware contained in an instruction memory is successively accessed and decoded by the instruction decoder to generate various control commands. Of relevance here are the MAC-CONTROLS which, by way of a multiplexer 41, reach a multiply control logic block 40 that controls the operation of the functional units 11, 12 and the operation of associated muxes 51 for retrieving data from a data memory 50.

Returning to the multiplexer 41, note that it is controlled by the mode bit 34 that was previously reset by the control pipeline. Whenever the value of the mode bit 34 is such that the FSM 32 is disabled, therefore, then the multiplexer 41 is controlled such that it transmits MAC-CONTROLS from the control pipeline 31 and not from the FSM 32. In the preferred embodiment, however, the instruction set is extended to include a special instruction (e.g. "Start FSM") which starts the FSM by setting the mode bit 34. At the same time, therefore, the mode bit 34 selects the FSM input of the multiplexer 41 such that it is the FSM 32 and not the control pipeline 31 that controls the functional units 11, 12. In the preferred embodiment, the FSM returns control to the control pipeline 31 after having completed its specialized task by way of an interrupt line 37. The "Start FSM" instruction may simply return control or it may, of course, include other parameters such as a predetermined location at which to continue execution.

It should be understood that there are many possible ways to implement the dynamic swapping of control, the system of Figure 2 being merely one example.

CLAIMS

I Claim:

1. A method of controlling data flow in a computer system, the method comprising:

selectively accessing, by an instruction decoder, at least one of a plurality of functional units of a processing unit;

selectively accessing, by a finite state machine, at least one of the plurality of functional units of the processing unit; and

dynamically assigning the instruction decoder and the finite state machine to access at least one of the plurality of functional units of the processing unit to control the flow of data in the computer system.

2. The method of claim 1 further comprising the instruction decoder controlling at least a portion of the data flow in the computer system and passing said control of the data flow in the computer system to the finite state machine according to instructions in the computer system.

3. The method of claim 1 wherein the at least one functional unit selectively accessed by the finite state machine is a specialized functional unit.

4. The method of claim 1 wherein the at least one functional unit selectively accessed by the instruction decoder is a general purpose execution unit.

5. The method of claim 1 further comprising the finite state machine controlling at least a portion of the data flow in the computer system and passing said control of the data flow in the computer system to the instruction decoder according to instructions in the computer system.

6. A processing architecture comprising:

a processing unit having at least one functional unit disposed therein;

a first control mechanism that is configured to control flow of data in one or more of the at least one functional units of the processing unit;

a second control mechanism that is configured to control flow of data in one or more of the at least one functional units of the processing unit; and

a processor configured to dynamically assign either the first or second control mechanisms to at least one functional unit of the processing unit.

7. The processing architecture of claim 6 wherein the first control mechanism controls at least a portion of the data flow in the processing architecture and passes said control of the data flow in the processing architecture to the second control mechanism according to instructions in the processing architecture.

8. The processing architecture of claim 6 wherein the at least one functional unit of the processing unit is a specialized functional unit.

9. The processing architecture of claim 6 wherein the at least one functional unit of the processing unit is a general purpose execution unit.

10. The processing architecture of claim 6 wherein the first control mechanism comprises an instruction-decoder.

11. The processing architecture of claim 6 wherein the second control mechanism comprises a finite state machine.

12. The processing architecture of claim 6 wherein the second control mechanism controls at least a portion of the data flow in the processing architecture and passes said

control of the data flow in the processing architecture to the first control mechanism according to instructions in the processing architecture.

13. A multiprocessor integrated chip comprising:

a processing unit having a plurality of functional units;

a controller including an instruction decoder and a finite state machine, the controller issuing a plurality of control signals according to operations of the instruction decoder and/or the finite state machine; and

the controller configured to dynamically assign the control signals from the controller to the processing unit.

14. The multiprocessor integrated chip of claim 13 wherein the controller further comprises a multiplexor that enables the instruction decoder to pass control of the processing unit to the finite state machine.

15. The multiprocessor integrated chip of claim 13 wherein the finite state machine of the controller interoperates with one of the functional units of the processing unit, the one of the functional units comprising a specialized functional unit.

16. The multiprocessor integrated chip of claim 13 wherein the controller dynamically assigns the control signals to the processing unit according to a first input signal received from the instruction decoder and a second input signal received from the finite state machine.

17. The multiprocessor integrated chip of claim 16 further comprising a control register having a mode bit that may be set by an instruction executing in the instruction decoder and reset by the finite state machine.

18. The multiprocessor integrated chip of claim 13 wherein at least one of the plurality of functional units of the processing unit comprises a specialized functional unit.

19. The multiprocessor integrated chip of claim 13 wherein at least one of the plurality of functional units of the processing unit comprises a general purpose execution unit.

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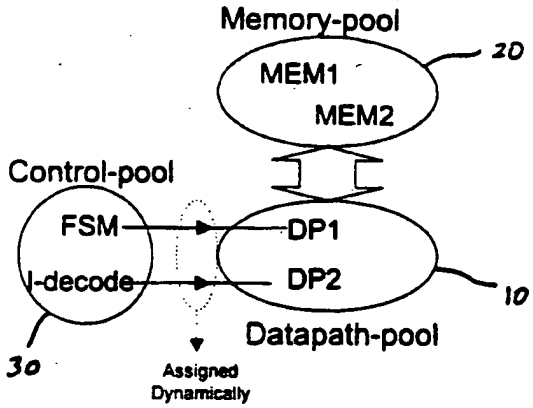
Memory-pool
MEM1
MEM2
20
Control-pool
FSM
I-decode
DP1
DP2
10
Datapath-pool
30
Assigned
Dynamically

FIG. 1

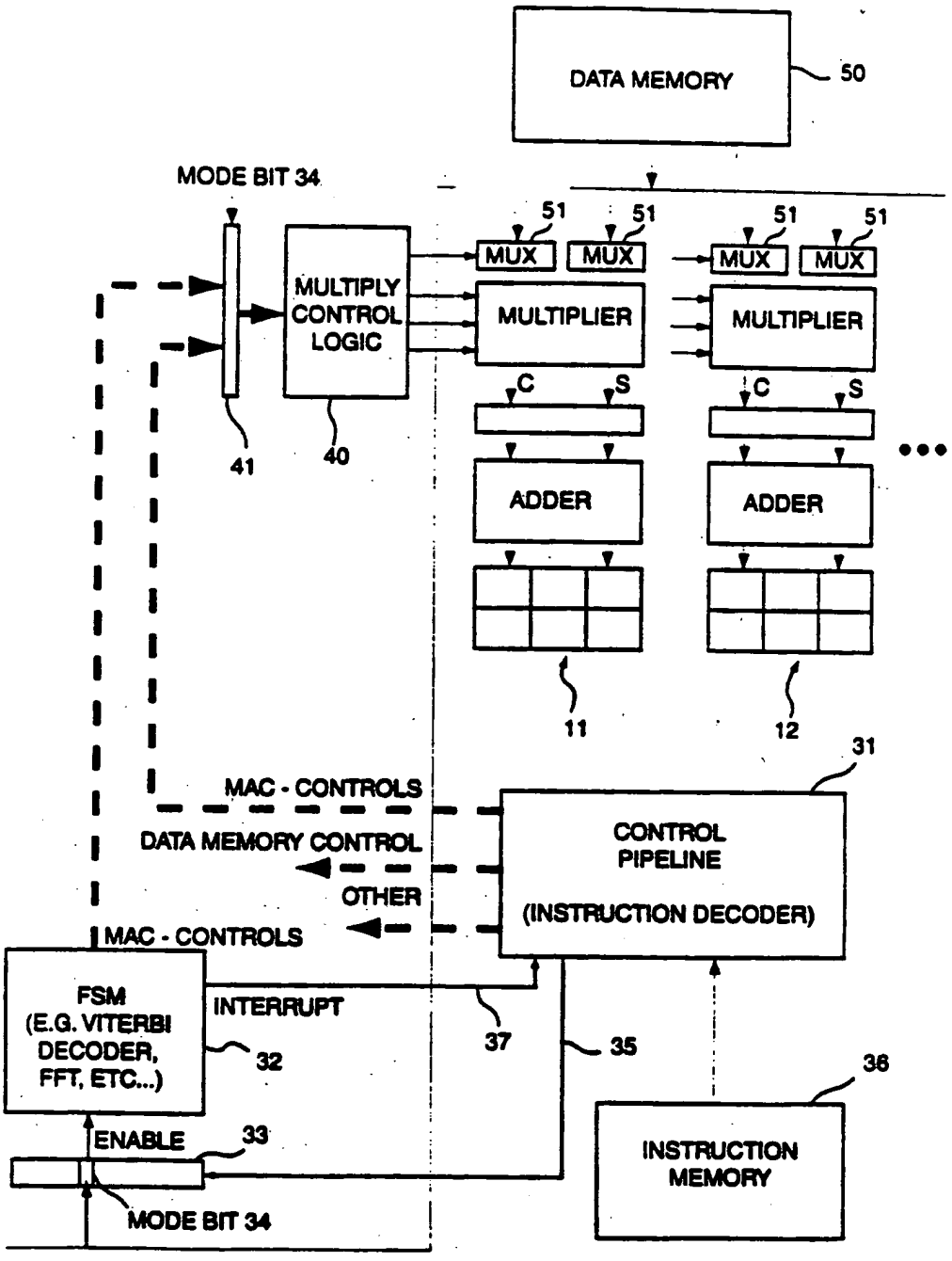
DATA MEMORY
50
MODE BIT 34
51
51
51
51
MUX
MUX
MUX
MUX
MULTIPLY CONTROL LOGIC
MULTIPLIER
MULTIPLIER
C
S
C
S
ADDER
ADDER
41
40
11
12
31
MAC - CONTROLS
DATA MEMORY CONTROL
OTHER
MAC - CONTROLS
CONTROL PIPELINE
(INSTRUCTION DECODER)
FSM (E.G. VITERBI DECODER, FFT, ETC...)
INTERRUPT
32
37
35
36
ENABLE
33
INSTRUCTION MEMORY
MODE BIT 34

FIG. 2

INTERNATIONAL SEARCH REPORT

Inte. onal Application No
PCT/US 99/22551

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/318 G06F9/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	US 5 864 689 A (TRAN THANG M) 26 January 1999 (1999-01-26) column 2, line 15 - line 54 column 3, line 61 -column 4, line 65 column 5, line 42 - line 60 column 8, line 31 -column 11, line 15	1-19
X	MOSER C W: "INCREASING AN INSTRUCTION SET WITHOUT INCREASING WORD LENGTH" ELECTRONICS, vol. 48, no. 3, - 6 February 1975 (1975-02-06) pages 114-115, XP002030199 US	6,7,9,10
A	the whole document	1,2,4,5, 8,11,13, 14,16,17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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26 January 2000	01/02/2000

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PCT/US 99/22551

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	the whole document	1-5,7,8, 11-19
A	"SELECTING PREDECODED INSTRUCTIONS WITH A SURROGATE" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 36, no. 6A, June 1993 (1993-06), page 35-38 XP000370750 ISSN: 0018-8689 the whole document	1-19

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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